DEI Analysis of an OTP EPROM

Dynamic Electroluminescence Imaging (DEI) applied to an OTP EPROM memory device

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Abstract:

DEI is an important non-invasive technique for the characterization of CMOS microelectronic circuits. Timing diagrams can be prepared from measurements of the luminescence transients that accompany the switching of transistors in operating devices without actually contacting internal circuitry. We report reverse engineering and timing measurements made on a 512K-bit EPROM enabled by the use of optical methods alone. The results demonstrate timing information with up to 11 ps time resolution that is correlated with the chip circuitry.

Introductory:

DEI was first applied to the imaging of operating CMOS circuits by a group at IBM [1,2]. They have successfully developed their use of DEI for circuit analysis and given it the acronym PICA (Picosecond Imaging Circuit Analysis). A commercial instrument incorporating this technique has been available since 2001.

Our equipment to observe DEI has been constructed with commercially available components. This instrument comprises a Karl Süss probe station equipped with a position-dissecting photomultiplier tube called a MEPSICRON™. This device counts individual photons and determines image {x,y,t} coordinates for each. McMullen et al. first described operation of this detector in this way in 1987 [3].

The Experiment:

DEI allows timing information to be collected at individual transistors in a circuit without directly probing the devices. To demonstrate the power of the technique a 512K-bit EPROM in ~1 micron technology was prepared for DEI measurement and operated by setting address lines A1 to A15 and the chip and output enable inputs low and driving the address line A0 directly with a pulse generator.

The EPROM circuitry was exposed for DEI measurement by decapsulating the part with acids. The circuitry was constructed with only two layers of metal so that optical observation from the front side was not problematic. Had there been multiple metal layers on the processed side then the part would have had to have been observed from the backside and this would have required

substantial die thinning to 50 µm or less. Figure 1 shows DEI images recorded: a) in the region of the tri-state drivers for bond pads D0 to D3 and b) in the region of bond pad D0.

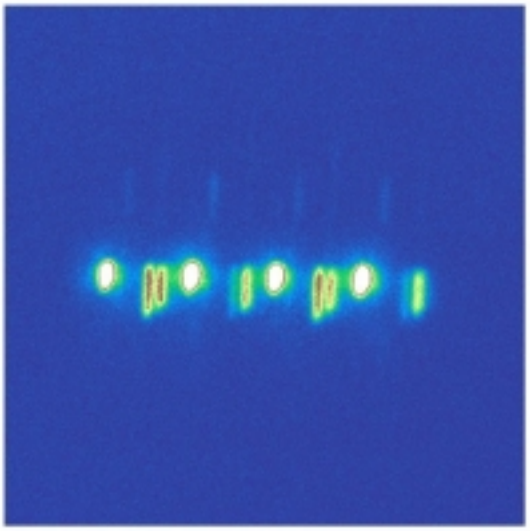

Figure 1a. The MX27C521pc-12 DEI from the tri-state drivers of the D0 to D3 bond pads. The four drivers are side by side. Each driver consists of a NAND gate on the left and a NOR gate on the right. The nFETs of these gates are below centre, the pFETs the faint luminescences above.

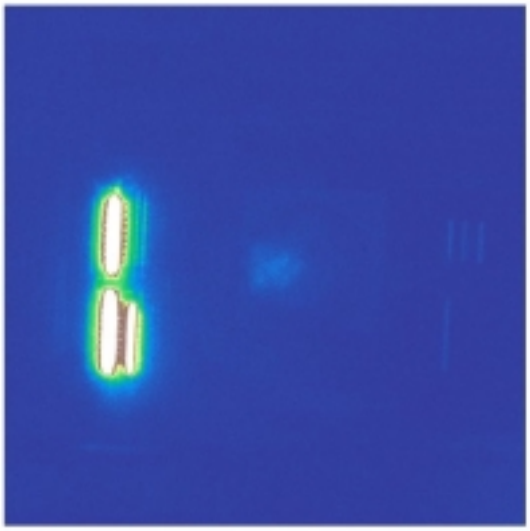

Figure 1b. The MX27C521pc-12 DEI from the region about the D0 bond pad with very bright nFET luminescence on the left, the bond wire imaged in reflected luminescence from the nFET in the centre and luminescence from the pFET faintly visible on the right.

Tri-state Drivers:

Figure 2 shows a dissection of the luminescence from the driver for the D0 bond pad. Referring to the figure, each tri-state driver consists of a separate circuit for the pFET and the nFET of the bond pad buffer. The data signal, D, coming from the column decoders is NANDed with a control signal, C, derived from the output enable input, producing Zp that is used to drive the output inverter pFET and NORed with the complement of the control signal, $\overline{C}$, producing Zn that is used to drive the nFET. The output enable input to the chip is held at DC and so the only switching occurs on the data line. The NAND has two nFETs in series, one driven by D and the other by C. Since C is always high, only the nFET driven by D changes state. This is the single very bright spot in the nFET region of each NAND gate. On the other hand, the nFETs of the NOR gates are connected in parallel. There are two finger-like luminescences in the nFET region of each NOR gate. As D goes high, only one conducts but as D goes low there is a luminescence transient from both nFETS.

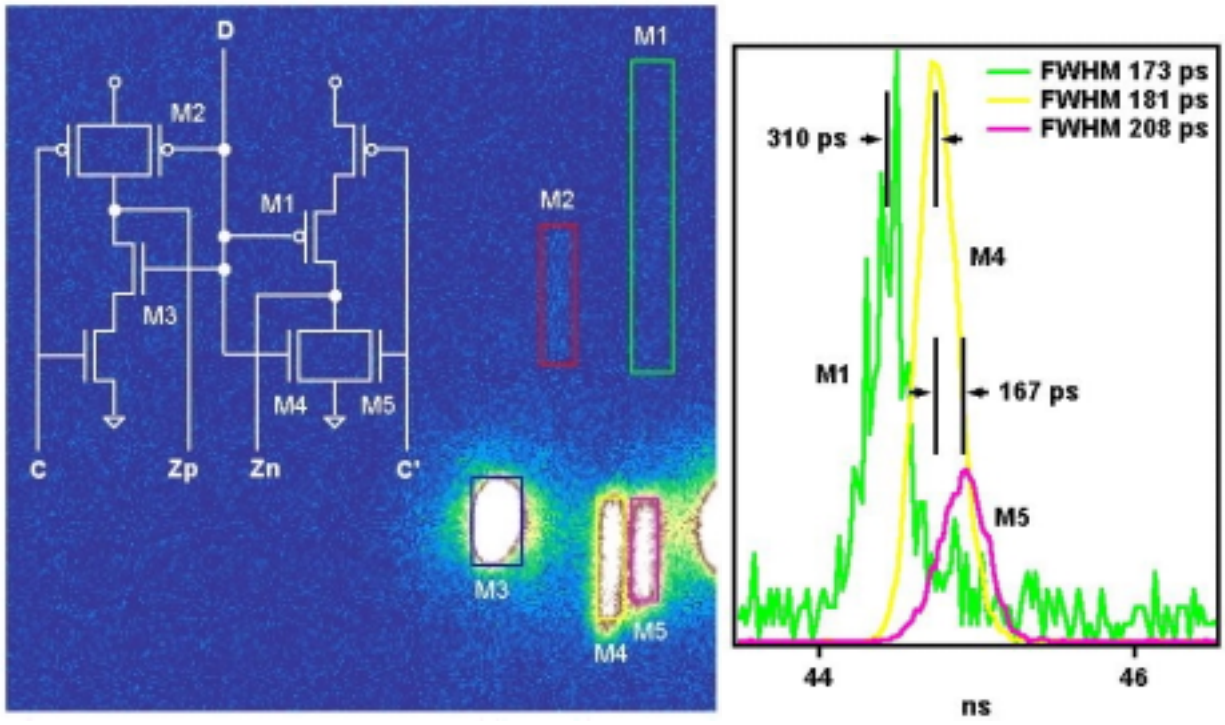

Figure 2. This dissection of a small portion of the image from Figure 1a shows the luminescence from the components of the tri-state driver for the D0 bond pad. The plot compares the waveforms for the visible NOR FETs.

D0 Bond Pad:

The tri-state driver output signals propagate to the bond pad buffer FETs in 3 ns. The luminescence from the bond pad nFET is particularly bright and broad, with a FWHM of 670 ps. Interesting is that the propagation of the signal to the three fingers of the nFET can be observed. Referring to figure 1b, the signal comes in on metal directly to the upper finger, passes on in metal to the left lower finger and then passes further in poly-silicon to the right lower finger. There is a reproducibly measurable delay of 11 ps from the upper finger to the left lower finger and then a further 27 ps to the right lower finger.

Summary:

DEI is a non-invasive means of obtaining an enormous amount of high-resolution timing information from a CMOS circuit. Obvious applications are non-invasive performance evaluation, failure analysis, IP evaluation and prototype testing. Moreover, in many modern devices that use a flip-chip mounting backside optical techniques are the methods of choice for probing circuitry.

References:

1. Tsang, J.C. and J.A. Kash, Appl. Phys. Lett. **70**, 889 (1997).
2. Tsang, J.C., J.A. Kash and D.P. Vallett, IBM J. Res. Develop. **44**, 583 (2000).
3. McMullen, W.G., S. Charbonneau and M.L.W.Thewalt, Rev. Sci. Instrum. **58**, 1626 (1987).