Printed Circuit Board Reliability and Integrity Characterization Using MAJIC

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Abstract
The recent need to develop lead-free electrical and electronic products has resulted in an increased demand to characterize solder joint integrity. Many standards exist to evaluate the long term reliability of electronic components or the quality of an assembly process. However no standards apply to custom printed circuit board assemblies. For example, the IPC-9701 standard and the use of evaluation boards are intended at evaluating processes as opposed to products. We have devised a methodology, combining inspection, the application of thermal and mechanical fatigue to stress the solder joints and the devices, and cross-section analysis to evaluate the quality of the solder joints, plated through-holes, and board manufacturing. This test, which we have named MAJIC (MuAnalysis Joint Integrity Characterization), has been applied to printed circuit boards of various finishes that have been assembled using leaded or unleaded solder pastes and using both leaded and unleaded components in various combinations.

The MAJIC methodology provides a vehicle to qualify an assembly process or to evaluate a supplier. With the addition of predetermined quantitative criteria, it could become a standard for the qualification of custom printed circuit board assemblies. This paper will demonstrate the wealth of information and reliability risks that have been exposed using this methodology on several products.

Introduction
Within the MAJIC methodology, inspired somewhat by the Telcordia approach, all tests and inspections are done according to exiting IPC, JEDEC or MIL-STD- 883 standards. Results are presented detailing the morphology of the solder joints with respect to intermetallic formation, wetting, cracking and voiding. Additional results reveal board and component reliability challenges in view of the additional thermal budget of lead free soldering.

Surface mount devices and BGA components are thus inspected with XRAY imaging, optical microscopy and acoustic microscopy before mechanical stress, and optical inspection is repeated after stressing. Cross-section analysis is then performed on selected components, active and passive, including plated through-holes. The cross-sections are analyzed by optical and electron microscopy, including EDX analysis.

MAJIC
The MAJIC test is designed to be stressing, but non destructive, and uses several components of JEDEC reliability tests. It consists of three parts: inspection, stress, and cross-section.

Inspection:
First the assembled boards are examined carefully for manufacturing defects according to or exceeding the IPC-A-610D standard. BGA or QFN components are imaged by X-Ray to detect gross defects in the solder joints. Semiconductor components are inspected by acoustic microscopy for evidence of delamination, since the reflow temperature is higher in lead-free soldering.

Stress:
Next the boards are stressed. Temperature cycling expands and contracts the solder joints without creation of intermetallics. The conditions are those of JEDEC JESD22-A104-B condition A: -55C to +85C, but, since the intention is only to reveal latent defects, only 10 cycles are applied.

Mechanical shock is then applied to the boards following the conditions of JESD22-B104-C. Condition A is used: 500G with a 1ms duration. Five shocks per direction (+x,-x,+y,-y,+z,-z) are applied for a total of 30 shocks.

Finally vibration is applied to the boards according to JESD22-B103-B. Condition 1 is used with a peak acceleration of 20G and a frequency sweep from 20 to 2000Hz.

The stressing imposed upon the boards in MAJIC is intended to fatigue the joints and reveal latent defects, not to destroy them. Following the application of these mechanical stresses acoustic microscopy is repeated on some of the critical components to determine if further delaminations have occurred. The visual inspection is also repeated to look for evidence of damage.

Cross-section:
Finally some of the devices are selected for cross-sectioning and microscopy, including EDX analysis.

Samples
We have applied MAJIC to a large variety of board, of different sizes and complexity. It has been used to compare processes on the same product (e.g. leaded vs lead-free), to evaluate or compare EMS suppliers, and to compare different component suppliers. RoHS component have been used with Sn/Pb solder and vice versa. Therefore the results presented here are not intended to demonstrate the superiority of one process over another or the compatibility of components and solder. They are meant to illustrate the types of latent defects and reliability exposure that have been revealed using the MAJIC approach.

Inspection results
Visual inspection:
The IPC-A-610D is very precise regarding how visual inspection should be performed. In lead-free soldering we have often found that some components cannot handle the extra heat. An example of a cracked diode is shown in Figure 1.

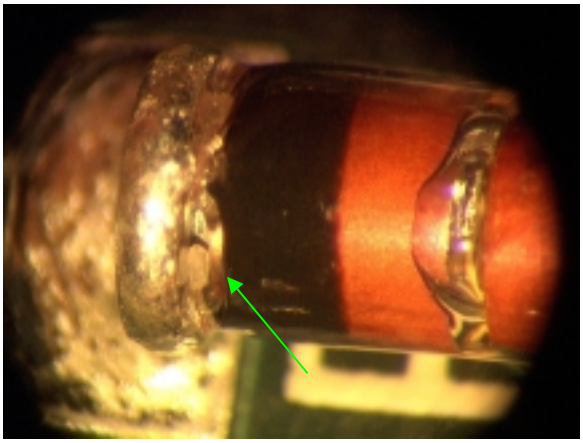


Figure 1 - A cracked diode.

Acoustic microscopy:
The extra thermal budget of lead free soldering is known to reduce the Moisture Sensitivity Level of plastic encapsulated ICs. Acoustic microscopy reveals if any delamination has occurred during the soldering process. ICs showing delamination can still test good electrically if the extent of the delamination is not severe and the wire bonds are still intact. However delamination is a latent defect that will reduce the long term reliability of the product. Eventually ionic contamination will cause bond pad corrosion or leakage. Evaluation boards often use dummy components without die and cannot detect such issues.

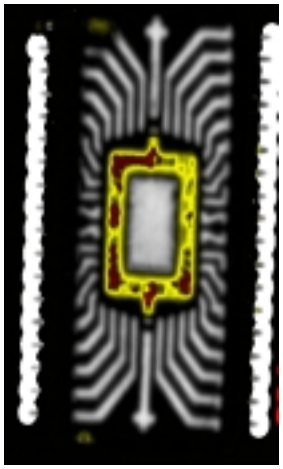


Figure 2 – An IC showing delamination of the lead- frame, revealed by Acoustic microscopy. This IC tested good electrically.

XRAY:
XRAY inspection is common in the industry to look at solder joints, particularly in BGAs and QFNs where the joint is hidden from sight. However it is time consuming and one must use high resolution to capture subtle wetting issues such as the ones shown in Figure3.

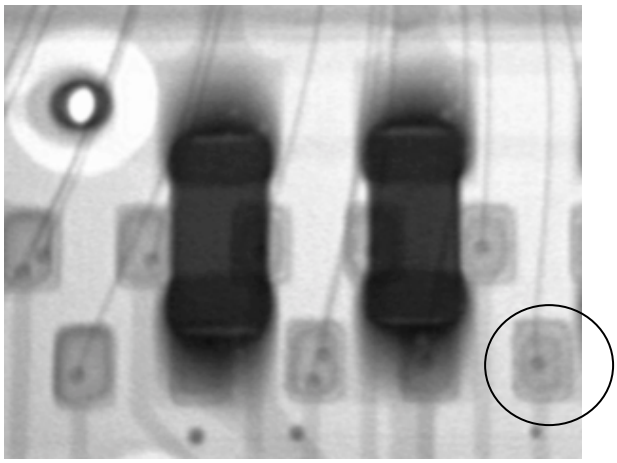
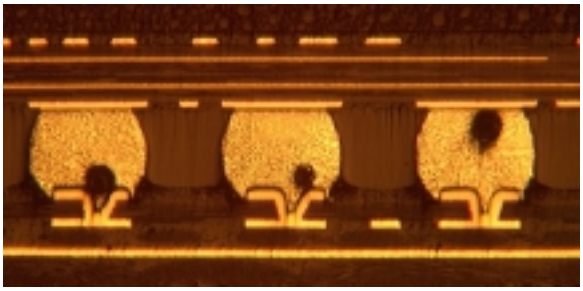


Figure 3 – Poor wetting and incomplete coverage of most of the solder pads in a QFN device. Only a small section of the device is shown. The worst pad is circled. The two discrete components in the field of view are on the other side of the board.

Cross-section results
After the stresses are applied, devices of each type are cross-sectioned and inspected with high resolution optical and electron microscopy. BGA balls are notorious for voids, which can usually be detected by XRAY. Different components can behave differently on the same board as shown in Figure 4, and cross-section analysis adds insight into the product quality assessment.



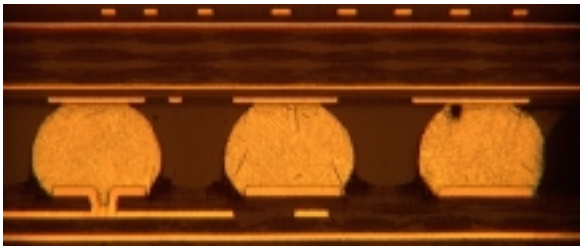


Figure 4 – BGA balls from two different components on the same product, showing significantly different voiding behavior.

Cracked capacitors are very difficult to detect at the board level. Although we have found that the capacitor of Figure 5 had cracked we could not detect the crack with acoustic microscopy. The geometry of the plates caused attenuation that hid the acoustic signal. Electrically this capacitor was still good since the crack had not reached the plates. Optically the crack could not be detected since it is within the solder filet and hidden from view. This capacitor would eventually fail electrically, damaging the product. It is not clear whether this capacitor failed because of heat or because of the mechanical stresses, but understanding that there is a reliability risk associated with this component, it is easy to devise experiments to figure out the root cause and address the issue.

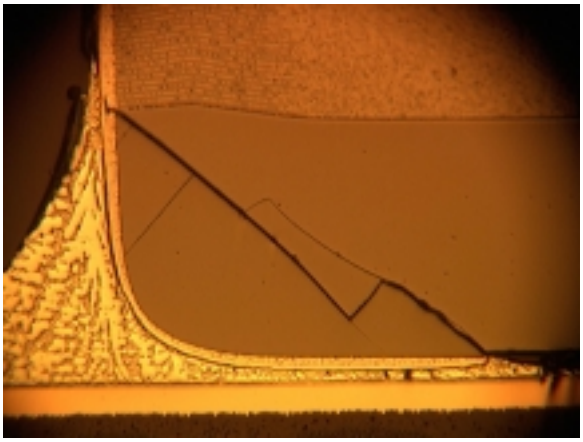


Figure 5 – Capacitor with crack that is invisible to optical inspection and acoustic microscopy.

Wetting problems should be detectable at visual inspection, but there are situations that elude detection. An example is shown in Figure 6: a gull wing component that looked good at visual inspection proved to be of poor quality after cross-section. It is likely that this solder joint will fail prematurely in the life of the product.

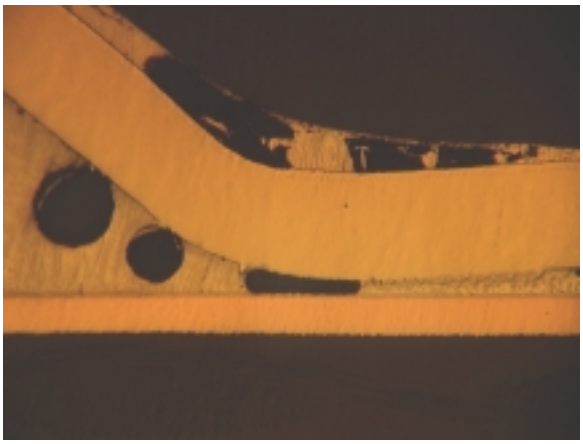


Figure 6 – Solder joint on gull wing component showing poor wetting, undetectable at visual inspection.

Plated through holes are very difficult to inspect. IPC-A-610D determines that the holes should be at least 75% filled. The pin of Figure 7 is very close to this figure of merit but, because of its location, the void could not be seen optically. In Figure 8, the pin passed visual inspection, but is it filled? Both these devices are likely to fail prematurely.

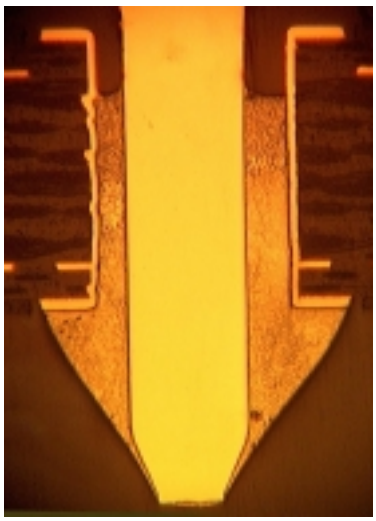


Figure 7- Pin in plated though via showing border line fill, not detectable by visual inspection because of location.

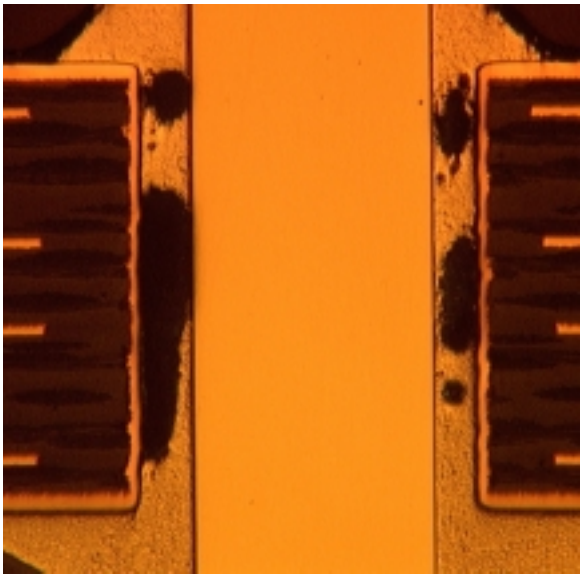


Figure 8 – Does this pin pass? It passed visual inspection.

There is more to manufacturing quality than solder joint integrity. How does one assess component cleanliness and handling? In the examples of Figures 9 and 10 we have observed voids and bubbles in the solder on the component side and all along a pin. Both these incidences occurred on the same board and the other components sectioned did not show anything abnormal. We suspect that the resistor and connector in question were contaminated. Perhaps they had been handled improperly or were received in a contaminated state.

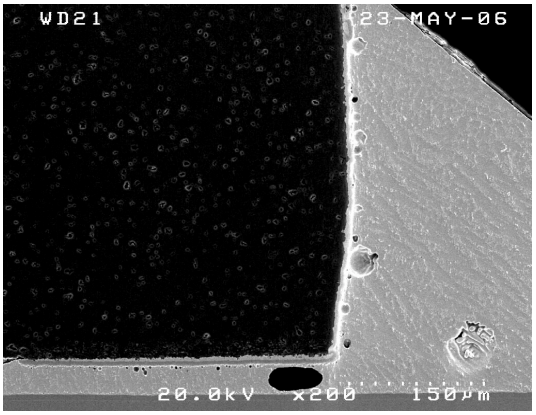


Figure 9 – Voids and bubbles on the component side of the solder joint of a resistor. It is possible that the component was contaminated.

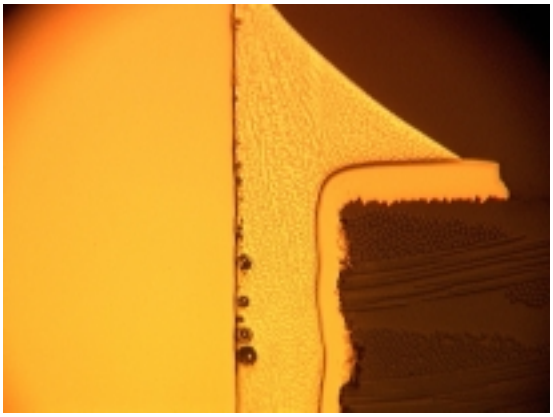


Figure 10 – Voids and bubbles in the solder joint along the pin of a connector. It is possible that the component was contaminated.

A significant area of concern and a frequently observed cause of failures in electronic products is the integrity of the printed circuit board itself. The best assembly process cannot compensate for board defects causing shorts, intermittents or opens. Electrical problems related to poor board construction do not occur immediately and are not necessarily detected at electrical testing. The latent defects will eventually become evident and cause failures for which the assembly manufacturer is likely to be blamed. The MAJIC stresses imposed on the product are not severe and should not cause cracking or delamination of a good board. However, if the board is improperly constructed, the stresses are likely to expose the flaws, particularly at cross-section where tiny defects can be seen by electron microscopy. Separation of the via barrel from the laminate, such as shown in Figure 11, is unfortunately very common and often leads to more severe damage including open circuits.

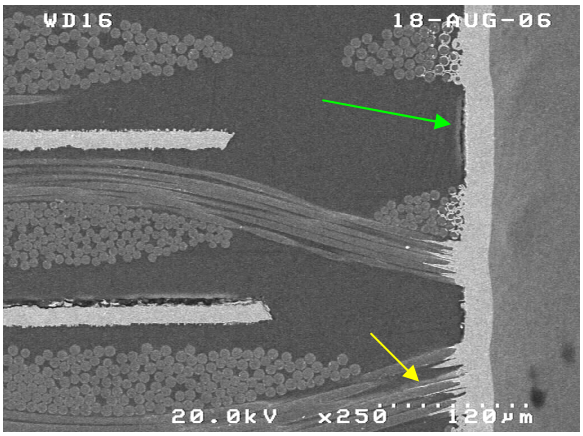


Figure 11- Cross-section of board showing separation between the laminate and the copper traces and the laminate and the copper barrel (green arrows). This board also exhibits significant copper wicking along the barrel of the via (yellow arrows).

EDX analysis

The last part of the MAJIC methodology is to examine the various compound/intermetallic phases created during the soldering process to ensure that proper reflow has occurred. Surprises, such as the unwanted presence of lead, may appear.

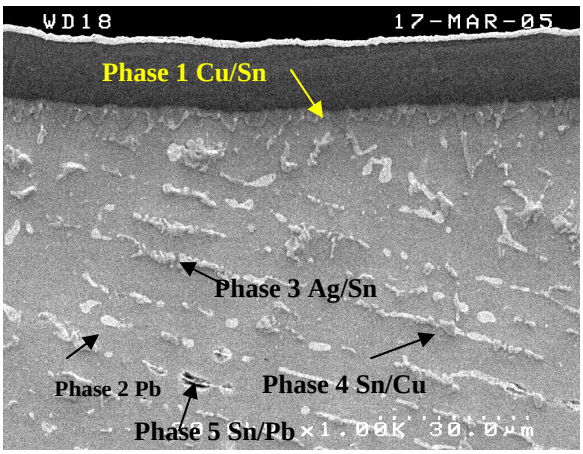


Figure 12 – EDX analysis shows the various compound/intermetallic phases present in this BGA ball cross-section.

Conclusion

A methodology, consisting of inspections and stresses designed to assess and document the quality of finished custom printed circuit board assemblies, has been presented. Several examples of latent defects, likely to cause premature product failure, that have been revealed using this methodology, have been demonstrated.

The stress conditions used were selected based on the complexity of the products and their applications. For example, military and aerospace applications may dictate different stressing conditions. Experimentation is required in order to optimize the stress conditions. Pass/fail criteria need to be established.

JEDEC and Telcordia each define series of tests to qualify electronic or optoelectronic components and modules. It is suggested that IPC follows suit and develops a qualification standard for custom printed circuit board assemblies. MAJIC should provide a good place to start.

Acknowledgements

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